CLAIM AMENDMENTS

Please cancel claims 25, 29 and 30 and amend claims 24 and 31, without prejudice, and adding new claims 32 – 41, all without prejudice, as indicated on the following listing of all the claims in the present application after this Amendment:

1 – 23. (cancelled)

24. (currently amended) A re-programmable non-volatile memory formed on a substrate, comprising:

a two-dimensional array of rows and columns of charge storage elements extending across the substrate in respective first and second directions that are orthogonal with each other,

discrete source and drain regions formed in the substrate between at least some of the charge storage elements in ~~one~~ the first direction and discontinuous in the second direction,

electrical isolation between the charge storage elements and the source and drain regions in the second direction, ~~and~~

first electrically conductive strips elongated in the second direction ~~and spaced apart in the first direction~~ across and in electrical contact with the source and drain regions, and spaced apart in the first direction,

second electrically conductive strips elongated in the second direction across and extending over columns of charge storage elements with field coupling therebetween, and

third electrically conductive strips elongated in the first direction across the first and second strips over rows of charge storage elements.

25. (cancelled)

26. (previously presented) The memory of claim 24, wherein the electrical isolation includes dielectric extending across the array in the first direction and between the charge storage elements and the source and drain regions in the second direction.

27. (previously presented) The memory of claim 26, wherein the electrical isolation additionally includes trenches in the substrate in which the dielectric is positioned.

28. (previously presented) The memory of claim 24, wherein the charge storage elements include conductive floating gates having a layer of dielectric between them and a surface of the substrate.

29. (cancelled)

30. (cancelled)

31. (currently amended) The memory of claim ~~29~~ 27, wherein the charge storage elements include conductive floating gates having a layer of dielectric between them and a surface of the substrate.

32. (new) The memory of claim 24, wherein the first strips have a thickness in excess of a combined thickness of neighboring charge storage elements and second strips thereover.

33. (new) The memory of claim 32, wherein the charge storage elements include conductive floating gates having a layer of dielectric between them and a surface of the substrate.

34. (new) A re-programmable non-volatile memory formed on a substrate, comprising:

a two-dimensional array of rows and columns of charge storage elements extending across the substrate in respective first and second directions that are orthogonal with each other,

discrete source and drain regions formed in the substrate between at least some of the charge storage elements in the first direction and discontinuous in the second direction,

electrical isolation between the charge storage elements and the source and drain regions in the second direction,

first electrically conductive strips elongated in the second direction across and in electrical contact with the source and drain regions, and spaced apart in the first direction,

second electrically conductive strips elongated in the second direction across and extending over columns of charge storage elements with field coupling therebetween, and

wherein the first strips have a thickness in excess of a combined thickness of neighboring charge storage elements and second strips thereover.

35. (new) The memory of claim 34, wherein the electrical isolation includes dielectric extending across the array in the first direction and between the charge storage elements and the source and drain regions in the second direction.

36. (new) The memory of claim 35, wherein the electrical isolation additionally includes trenches in the substrate in which the dielectric is positioned.

37. (new) The memory of claim 36, wherein the charge storage elements include conductive floating gates having a layer of dielectric between them and a surface of the substrate.

38. (new) The memory of claim 34, wherein the charge storage elements include conductive floating gates having a layer of dielectric between them and a surface of the substrate.

39. (new) An array of non-volatile memory cells on a semiconductor substrate, comprising:

a two-dimensional array of floating gates arranged in rows extending in a first direction across the substrate with spaces therebetween in a second direction and columns extending in the second direction across the substrate with spaces therebetween in the first direction, said first and second directions being orthogonal with each other, a first set of spaces separating the columns of floating gates including ones of every other space across the substrate in the first direction and a second set of spaces separating the columns of floating gates including remaining ones of every other space across the substrate in the first direction and in between the first set of spaces,

source and drain regions spaced apart in the first direction across the substrate along the rows and coincident with the first set of spaces between columns of floating gates,

elongated electrically conductive bit lines having lengths extending across the substrate in the second direction within the first set of spaces between columns of floating gates, said bit lines individually extending over and electrically contacting a plurality of said source and drain regions in adjacent rows,

elongated steering gates having lengths extending across the substrate in the second direction and being spaced apart in the first direction to overlay columns of floating gates with said second set of spaces positioned between adjacent steering gates,

elongated select gates having lengths extending across the substrate in the first direction over the bit lines and steering gates, and spaced apart in the second direction over rows of floating gates, said select gates extending into said second set of spaces,

wherein the source and drain regions are formed in the substrate and electrically isolated from one another in the second direction by strips of dielectric elongated in the first direction and positioned in the second direction between the rows of floating gates, and

wherein the bit lines have a thickness in excess of a combined thickness of neighboring floating and steering gates stacked on one another.

40. (new) The memory cell array of claim 39, wherein the strips of dielectric are formed in trenches in the substrate.

41. (new) The memory cell array of claim 39, wherein the first electrically conductive strips are formed of doped polycrystalline silicon.